What is claimed is:

1. A high-speed signal transmission system,

wherein a regulator circuit for reshaping a sending waveform by detecting and analyzing a defect relative to signal transmission of a line by a waveform analysis circuit is added to an output end so that the regulator circuit is adjusted to obtain a waveform in a good condition at a receiving end.

2. A high-speed signal transmission system according to claim 1, wherein said regulator circuit is adjusted by statistical search method.

3. A high-speed signal transmission system according to claim 2, wherein said statistical search method includes one or a combination of genetic algorithm, climbing-up method, annealing method, enumeration method, evolution policy, and taboo search method.

4. A high-speed signal transmission system according to claim 1, wherein said line is matched with a characteristic impedance from a sending end to a terminal end, a sense amp on the receiving end receives a mixture of the sending waveform and a total-reflection waveform, and a terminal resistance is inserted in the sending end so that the total-reflection waveform is not transmitted from the sending end through re-reflection.

5. A high-speed signal transmission system according to claim 1, wherein one of said sending end and the terminal end of the line is connected to a power source or ground for recognizing a reference potential, and the other of the sending end and the

terminal end opposite to the one of the sending end and the terminal end for recognizing the reference potential is not connected to the power source or the ground.

6. A high-speed signal transmission system according to claim 5, wherein a power-supply line of said system is formed of pair lines of the power source and ground, and one exclusive pair of lines is connected to an element circuit of each of minimum logic element circuits and memory element circuits.

7. A high-speed signal transmission system according to claim 5, wherein a sense amp at the terminal end is formed of a MOS-FET having a gate capacitance less than 10 fF.

8. A high-speed signal transmission system according to claim 5, wherein said line has a structure that a TEM mode is maintained.

9. A high-speed signal transmission system according to claim 5, wherein said line has a portion where an electromagnetic wave leaks into air, said portion being coated with a high permittivity material so that an effective permittivity of the portion matches a permittivity of an internal dielectric member.

10. A high-speed signal transmission system according to claim 5, wherein said line has one of a structure of a pair coplanar, stacked-pair, guard stacked-pair, and guard coplanar.

11. A high-speed signal transmission system according to claim 5, wherein said line has a relatively same physical structure throughout a whole line with an isometric wiring length based on

a parallel isometric wiring, and uses a circular wiring to make a fan-out wiring isometric when the line is composed of a plurality of bits.

12. A high-speed signal transmission system according to claim 5, wherein said line has a driver circuit and a receiver circuit formed of a MOS-FET of Si or SiGe, or an n-channel MES-FET of GaAs, and composed of a differential output circuit and differential input circuit without ground connection, a short-key high-speed bipolar differential circuit, or a bus-switch circuit.

13. A high-speed signal transmission system according to claim 12, wherein a varactor having a structure of one of a complementarily same MOS-FET, MES-FET, and a bipolar transistor is arranged in all transistors.

14. A high-speed signal transmission system according to claim 13, wherein said complementary operating element has a common well electrically floated.